REMARKS

Claims 10-36 are pending in the Application and all were rejected in the Office action mailed October 16, 2008. No claims are amended by this response. Claims 10 and 24 are independent claims, while claims 11-23 and 25-36 depend either directly or indirectly from independent claims 10 and 24, respectively. Applicants respectfully request reconsideration of claims 10-36, in light of the following remarks.

As an initial matter, Applicants respectfully note that the instant Office action indicates at Box 1 of the Summary that the Office action is responsive to communication(s) filed on "11 February 2008". Applicants respectfully submit that the most recent previous correspondence filed in the Application is Applicants' response filed September 10, 2008. Therefore, Applicants' assume that the Office is responding to the correspondence filed by the Applicants on September 10, 2008. Applicants respectfully request that the Office contact the undersigned if this is in error.

Applicants respectfully note that the Office cites Bruck (US 6,519,289) in at least the Office actions mailed April 10, 2008 and October 16, 2008, but that Bruck does not appear on any PTO-892 form of record. Applicants respectfully request that Bruck be made of record in the Application by its appearance on a PTO-892 form.

The Applicants note that a goal of patent examination is to provide a prompt and complete examination of a patent application.

> **It is essential** that patent applicants obtain a prompt yet complete examination of their applications. Under the principles of compact prosecution, **each claim should be reviewed for compliance with every statutory requirement for patentability in the initial review of the application**, even if one or more claims are found to be deficient with respect to some statutory requirement. Thus, **USPTO personnel should state all reasons and bases for rejecting claims in the first Office action**. Deficiencies should be explained clearly, particularly when they serve as a basis for a rejection. Whenever practicable, USPTO

> personnel should indicate how rejections may be overcome and how problems may be resolved. **A failure to follow this approach can lead to unnecessary delays in the prosecution of the application**.

M.P.E.P. §2106(II) (emphasis added).

As such, the Applicants assume, based on the goals of patent examination noted above, that the current Office Action sets forth "all reasons and bases" for rejecting the claims.

Applicants respectfully note that no claims are amended by this response. However, Applicants respectfully submit that the Office has again misinterpreted the teachings of the cited references, and respectfully request that the cited references and the following remarks be thoroughly considered by the Office, to avoid the need to proceed to appeal.

Rejection of Claims

Claims 10-20 and 24-33 were rejected under 35 U.S.C. §102(e) as being anticipated by Hinchley, et al. (US 6,490,250, hereinafter "Hinchley"). Claims 21-22 and 34-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley in view of Ishihara, et al. (US 6,516,031, hereinafter "Ishihara"). Claims 23 and 36 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley in view of Ishihara, and further in view of Kopet, et al. (US 5,448,310, hereinafter "Kopet").

The Office also rejects claims 10-12, 15-16, 20, 24-25, 28-29, and 33 under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy, et al. (US 6,665,872, hereinafter "Krishnamurthy"). Claims 13 and 26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy in view of Bruck. Claims 14, 17-19, 27, and 30-32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy in view of Hinchley. Claims 21-22 and 34-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy in view of Boice, et al. (US 6,823,013, hereinafter "Boice"). Claim 23 appears to have been rejected under 35 U.S.C. 103(a)

as being unpatentable over Krishnamurthy in view of Boice, and further in view of Kopet.

Applicants respectfully traverse the rejections for at least the reasons set forth during prior prosecution, in addition to those set forth below.

I. Hinchley Does Not Anticipate Claims 10-20 And 24-33

Claims 10-20 and 24-33 were rejected under 35 U.S.C. §102(e) as being anticipated by Hinchley.

With regard to the anticipation rejections, MPEP 2131 states, "[a] claim is anticipated **only** if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). MPEP 2131 also states, "[t]he identical invention **must** be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). (emphasis added)

Applicants' independent claim 10 recites, in part, "[a] single-chip audio/video encoder device comprising, on a single integrated circuit: multiplexer circuitry that operates in a first mode and a second mode, which when operating in the **first mode** produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the **second mode** concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio;...." Applicants respectfully submit that Hinchley does not teach or suggest at least these aspects of Applicants' claim 10.

The Office states at pages 2-3 that Hinchley teaches:

> multiplexer circuitry *(200 of fig. 2, 750 of fig. 7)* that operates in a first mode and a second mode *(Column 6, lines 12-16; Note Hinchley discloses MUX logic 750 which*

> *performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined (multiplexed) multimedia stream (audio and video) 224, which is similar to the multiplexing circuit as disclosed in paragraph [0063] of the present invention publication (US 20041016103 2 A1))*, which when operating in the first mode produces a first multiplexed stream (first combined multimedia stream, 224 of fig. 7) from first compressed video, first compressed audio , second compressed video, and second compressed audio (208 of fig. 2; MPEG-2 standard encoders for encoding video and audio); and which when operating in the second mode concurrently produces the first multiplexed stream (224 of fig. 7) from the first compressed video and the first compressed audio, and produces a second multiplexed stream (224 of fig . 7) from the second compressed video and the second compressed audio (208 of fig. 2; MPEG-2 encoders for encoding the second video and second audio);...

(italics in original)

The Office cites elements "200", "208", and "224" of Fig. 2, elements "224" and "750" of Fig. 7, and col. 6, lines 12-16 of Hinchley as teaching this aspect of Applicants' claim 10. Applicants respectfully submit that a review of Figs. 2 and 7 of Hinchley shows that there is nothing in either figure that teaches or suggests "multiplexer circuitry" that operates in a "first mode" and "second mode", as claimed. Hinchley identifies element "200" as "stream processor 200", element "208" as "multimedia encoder 208", and element "224" as "combined multimedia stream/output combined data 224". Hinchley states that "...stream processor 200 retrieves data on data line 240 from the unified memory module 204 and processes the data in accordance with a linked list of commands comprising dedicated instructions for multiplexing the data into **a single output stream** 224." *See id.* at col. 4, lines 9-13. Hinchley goes on to say that "[t]he combined stream data 224 is stored back into the unified memory module 204. Bus 122 is used to access the combined stream data 224 for transmission to other components of the system 100." *Id.* at col. 4, lines 14-17. Thus, Hinchley clearly

explains that the "stream processor 200" produces a "**single** output stream 224" that is stored into the "unified memory module 204".

Therefore, for at least these reasons, Applicants respectfully submit that the cited portions of Hinchley fail to teach "multiplexer circuitry" that produces a "first multiplexed stream" while operating in the "first mode" **and** that produces a "first multiplexed stream" **and** a "second multiplexed stream", while operating in a "second mode", and wherein the device "...transmits the first multiplexed stream to circuitry external to the device via a first output of the device..." **and** "...transmits the second multiplexed stream to circuitry external to the device via a second output of the device", as claimed.

Applicants respectfully submit that mere disclosure of "MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined (multiplexed) multimedia stream (audio and video) 224", as asserted by the Office, is quite different from and does not teach or suggest the patentably distinct operation in accordance with Applicants' "first mode" and "second mode", as claimed. Indeed, Applicants respectfully submit that Hinchley fails to show any recognition of the utility of such operation, let alone provide any teachings in this regard. Hinchley clearly fails to teach or suggest producing "a first multiplexed stream" **and** "a second multiplexed stream" wherein "the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device" **and** "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device", as claimed. Applicants respectfully note that "[a] claim is anticipated **only** if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," and that "[t]he identical invention **must** be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. §2131. For at least the above reasons, Applicants respectfully submit that Hinchley does not teach each and every element of Applicants' claim 10, and that claim 10 is allowable over Hinchley.

Applicants' claim 10 is allowable for additional reasons. Applicants' independent claim 10 also recites, in part, "a first encoder that receives first uncompressed video

data **and** first uncompressed audio data, and that produces the first compressed video **and** the first compressed audio;..." and "...a second encoder that receives second uncompressed video data **and** second uncompressed audio data, and that produces the second compressed video **and** the second compressed audio;...." Applicants respectfully submit that Hinchley does not teach or suggest at least this aspect of Applicants' claim 10.

The instant Office action states that Hinchley teaches, in part at page 3:

> a first encoder (208 of fig. 2, see also fig. 3, the encoder (208 of fig. 2) supports the MPEG-2 standards; col. 3, lines 32-38; which is similar to the encoder of the present invention publication (US 200410161032 A1) as shown in paragraph [0036]) that receives first uncompressed video data and first uncompressed audio data (108 of fig. 2), and that produces the first compressed video and the first compressed audio;
>
> a second encoder *(208 of fig. 2; the encoder (208 of fig. 2) supports the MPEG-2 standards; col. 3, lines 32-38; which is similar to the encoder of the present invention publication (US 200410161032 Al) as shown in paragraph [00361)* that receives second uncompressed video data and second uncompressed audio data (108 of fig. 2), and that produces the second compressed video and the second compressed audio;

(italics in original)

Applicants respectfully disagree. The Office identifies "multimedia encoder 208" of Fig. 2 of Hinchley as teaching each of Applicants' "first encoder" and "second encoder". Claim 10 recites a "first encoder that receives first uncompressed video data **and** first uncompressed audio data," and "produces the first compressed video **and** the first compressed audio," and a "second encoder that receives second uncompressed video data **and** second uncompressed audio data, and that produces the second compressed video **and** the second compressed audio." Thus, Applicants' claim recites two encoder that **each** compress video **and** audio to produce compressed video **and** compressed audio.

Hinchley describes "multimedia encoder 208" at col. 4, lines 18-29, which state:

> FIG. 3 is a more detailed block diagram of one embodiment of the multimedia encoder 208 in accordance with the present invention. Compression engine 312 encodes incoming video frames 230 into a video elementary stream **or** audio samples 230 into an audio elementary stream. The output compressed elementary multimedia stream 316 is transmitted to an adjustable delay engine 300. The adjustable delay engine 300 adjusts the data rate of the compressed elementary multimedia stream 316 responsive to the data rate feedback signal 212, 214 received from the multimedia processor 250. The adjusted elementary multimedia streams 216, 218 are transmitted to the unified memory module 204.

(emphasis added)

Fig. 3 of Hinchley shows only one "compression engine 312", and clearly states above that "compression engine 312 encodes incoming video frames 230 into a video elementary stream **or** audio samples 230 into an audio elementary stream." Thus Hinchley teaches two "elementary streams" - an "audio elementary stream" and a "video elementary stream". Hinchley states, at col. 1, lines 13-25:

> Conventional MPEG encoders typically use two encoders, video and audio, which receive data transmitted from a data source. Each encoder is coupled to a separate memory for storing the video and audio data. The video encoder compresses the video data and transmits the compressed data to the conventional stream multiplexer controller. The audio encoder performs the same tasks and transmits the compressed audio data to the stream multiplexer controller. In an MPEG2 environment, the two elementary streams are multiplexed by the stream multiplexer controller to generate either a Program or Transport stream, depending on the embodiment."

(emphasis added)

Thus, Hinchley clearly uses the term "elementary stream" to refer to either a stream of audio data **or** a stream of video data, but does not use the term to refer to combined audio and video. In addition, Applicants respectfully submit that Hinchley

teaches that each of the "multimedia encoder 208" of Fig. 2 encodes **either** an "elementary stream" of "audio data", **or** an "elementary stream" of "video data," **but not both**. Therefore, the "multimedia encoder 208" of Hinchley, which has been identified by the Office as teaching Applicants' claim elements "first encoder" and "second encoder", does not teach or suggest **either** of Applicants' "first encoder" and "second encoder" that each receive uncompressed video data and uncompressed audio data and produce compressed video and compressed audio, in accordance with Applicants' claim 10. To the extent that the Office may suggest that one of the "multimedia encoder 208" of Fig. 2 may be used to encode an "elementary stream" of "audio data" and the second of Hinchley's "multimedia encoder 208" be used to encode an "elementary stream" of "video data", Applicants respectfully submit that such an arrangement only functions similar to one of Applicants' claimed "first encoder" and "second encoder". Applicants again respectfully note that "[a] claim is anticipated **only** if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," and that "[t]he identical invention **must** be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. §2131.

Further, Fig. 2 of Hinchley shows only two of "multimedia encoder 208", and even if Applicants agreed that Hinchley disclosed a greater number of "multimedia encoder 208", which Applicants do not, Hinchley offers no teaching or suggestion of operating the "integrated multimedia encoding system 120" of Fig. 2 in accordance with Applicants' "first mode" and "second mode", as claimed. Therefore, Applicants respectfully submit that the "multimedia encoder 208" of Hinchley does not teach Applicants' "a first encoder that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;..." **and** "...a second encoder that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;...,"as claimed, and that Hinchley does not anticipate Applicants' claim 10 for at least this additional reason.

Applicants respectfully submit that Applicants' claim 10 is allowable over Hinchley for additional reasons. Applicants' claim 10 recites, in part, "...control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder." The Office action states, at page 4:

> control circuitry *(250 of fig. 2, the multimedia processor is designed to perform multimedia operations as well as specialized functions, which is similar to the global controller (104) of the present invention publication (US 200410161032 A1) as shown in paragraph [0050]; the MPEG-2 inherently has the control function to synchronize the multiplexer, audio and video encoder together, since Hinchley discloses MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined (multiplexed) multimedia stream (audio and video) 224 and controller 250 for synchronize the multiplexer, and audio and video encoders according to the MPEG-2 standards))* that synchronizes (**harmonizes, coordinates, or orchestrates**) the multiplexing circuitry (200 of fig. 2; col. 7), the first encoder, and the second encoder (208 of fig. 2);...
>
> (italics and bold in original)

Applicants respectfully submit that a review of Hinchley shows that the entirety of Hinchley fails to make any mention of "synchronization". Cited element "250" of Hinchley, which has been identified by the Office as teaching Applicants' element "control circuitry", is identified by Hinchley as "multimedia processor 250." (*See id.* at col. 3, line 50) Hinchley describes "multimedia processor 250" at col. 3, line 65 to col. 4, line 2 stating, "...[m]ultimedia processor 250 is preferably a Digital Signal Processing (DSP) core which is designed to perform conventional multimedia operations as well as the specialized functions in accordance with the present invention." Applicants respectfully submit that any portion or figure of Hinchley teaches or suggests that the "multimedia processor 250" "synchronizes", "harmonizes", "coordinates", or "orchestrates" anything, as asserted by the Office, let alone synchronizing the "multimedia encoder 208" and "stream processor 200" of Fig. 2, which have been

identified by the Office as teaching Applicants' claim elements "first/second encoder" and "multiplexer circuitry". The mere statement by the Office that "...MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2..." is not sufficient to *prima facie* establish that "multimedia processor 250" teaches Applicants' "...control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder...," as claimed. Therefore, Applicants respectfully submit that Hinchley fails to teach or suggest at least Applicants' feature "...control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder...," and that Hinchley fails to anticipate Applicants' claim 10 for at least this additional reason.

Based at least upon the above, Applicants respectfully submit that the Office has failed to show that Hinchley teaches each and every element of Applicants' claim 10, as required by M.P.E.P. §2131, that the Office has not established a *prima facie* case of anticipation, and that claim 10 is allowable over Hinchley. Applicants respectfully submit that claims 11-23 depend either directly or indirectly from allowable claim 10, and are therefore also allowable over Hinchley, for at least the same reasons.

With regard to independent claim 24, Applicants respectfully submit that claim 24 was rejected for the same reasons citing the same portions of the Hinchley reference presented for the rejection of claim 10. Therefore, Applicants respectfully submit that claim 24 is allowable over Hinchley, for at least some of the reasons set forth above with respect to claim 10. Further, because claims 25-36 depend from allowable claim 24, Applicants believe that claims 25-36 are also allowable over Hinchley, for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of claims 10-20 and 24-33 under 35 U.S.C. §102(e) be reconsidered and withdrawn.

II. The Proposed Combination Of Hinchley And Ishihara Does Not Render Claims 21, 22, 34, And 35 Unpatentable

Claims 21-22 and 34-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley in view of Ishihara. Applicants respectfully submit that claims 21 and 22 and claims 34 and 35 depend, respectively, from independent claims 10 and 24. Applicants respectfully submit that claims 10 and 24 are allowable over the proposed combination of references, in that the Office has not asserted that Ishihara remedies any of the shortcomings of Hinchley, set forth above with respect to claims 10 and 24. Applicants respectfully submit that because independent claims 10 and 24 are allowable over the proposed combination of Hinchley and Ishihara, claims 21, 22, 34, and 35 that depend therefrom are also allowable, for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of claims 21, 22, 34, and 35 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

III. The Proposed Combination Of Hinchley, Ishihara, And Kopet Does Not Render Claims 23 And 36 Unpatentable

Claims 23 and 36 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley in view of Ishihara and Kopet. Applicants respectfully submit that claims 23 and 36 depend, respectively, from independent claims 10 and 24. Applicants respectfully submit that claims 10 and 24 are allowable over the proposed combination of references, in that the Office has not asserted that Kopet remedies any of the shortcomings of Hinchley and Ishihara, set forth above. Applicants respectfully submit that because independent claims 10 and 24 are allowable over the proposed combination of references, claims 23 and 36 that depend therefrom are also allowable, for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of claims 23 and 36 U.S.C. §103(a) be reconsidered and withdrawn.

IV. Krishnamurthy Does Not Render Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 Unpatentable

Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy. Applicants respectfully note that the Office relies only upon Krishnamurthy in the rejection of claims 10-12, 15-16, 20, 24-25, 28-29, and 33. Applicants also respectfully note that the rejection that appears on pages 8-9 of the instant Office action is a verbatim copy of the rejection set forth on pages 3-4 of the Office action mailed April 10, 2008, to which Applicants responded on September 10, 2008.

With respect to the rejections under 35 U.S.C. §103(a), Applicants respectfully submit that the Office action has failed to establish a *prima facie* case of obviousness, in accordance with M.P.E.P. §2142. According to M.P.E.P. §2142, "[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." M.P.E.P. §2142 further states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." As recognized in M.P.E.P. §2142, "[t]he Supreme Court in *KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007), 82 USPQ2d 1385, 1396 noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit." In addition, the Federal Circuit has made clear that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). See also *KSR*, 127 S. Ct. 1727 (2007), 82 USPQ2d at 1396.

In addition, M.P.E.P. §2143.03 states:

> To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re* Royka, 490 F.2d 981, 180

> USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re* Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re* Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

(emphasis added)

Applicants again respectfully submit that, according to Krishnamurthy at column 1, lines 15-19, Krishnamurthy "...relates to the compression and transmission of video signals, and, in particular, to the compression and transmission of multiple compressed video streams over a **single**, shared communication channel." (emphasis added)

With regard to independent claim 10, Applicants respectfully maintain that claim 10 recites, in part, "...[a] single-chip audio/video encoder device comprising, on a single integrated circuit: multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio; ... wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device." Applicants respectfully maintain that Krishnamurthy does not teach or suggest at least these aspects of Applicants' claim 10.

Applicants again address the teachings of Fig. 3 of Krishnamurthy, many of the elements of which are cited by the Office. Fig. 3 of Krishnamurthy is reproduced below:

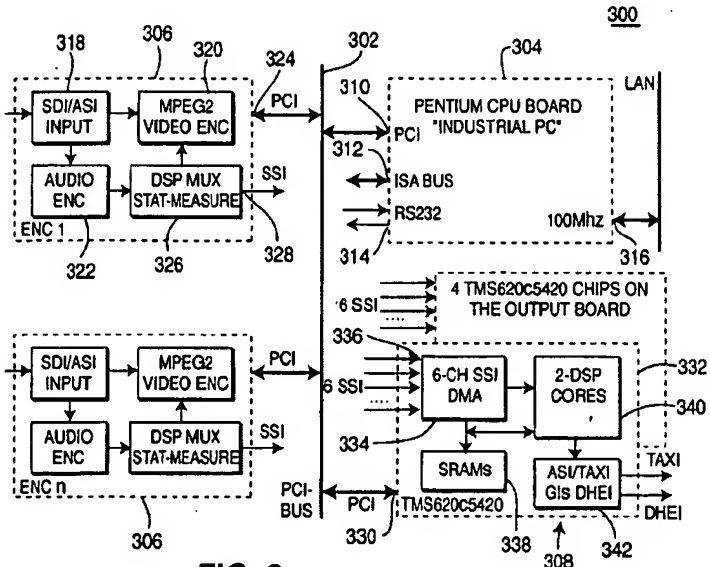

FIG. 3

Krishnamurthy teaches that Fig. 3 is "...a system-level block diagram of computer system, according to one embodiment of the present invention." *See id.* at column 4, lines 8-10. Krishnamurthy describes Fig. 3 in greater detail at column 18, lines 9-19, which is reproduced below:

> FIG. 3 shows a system-level block diagram of computer system 300, according to one embodiment of the present invention. Computer system 300 is a PCI bus-based industrial PC (Personal Computer) enclosure with multiple PCI boards. In particular, computer system 300 comprises a PCI bus 302 configured with a Central Processing Unit (CPU) board 304, up to n=24 encoder boards 306, and a statistical multiplexing (stat-mux) board 308. Although computer system 300 relies on a PCI bus, it will be understood that any other suitable system bus could be used in alternative embodiments of the present invention.

It is clear from Fig. 3 and the section of Krishnamurthy arguably the most relevant text portion of Krishnamurthy, that a "computer system" in accordance with an

embodiment of Krishnamurthy has a "central processing unit (CPU) board", a number of "encoder boards", and a "statistical multiplexing (stat-mux) board", and that it processes "multiple compressed video streams" for transmission "over a **single**, shared communication channel." Thus, Krishnamurthy states clearly that the multiplexed video/audio that is produced by the system of Krishnamurthy is transmitted over a **single** shared communication channel.

Applicants respectfully submit that the Office has not even addressed this aspect of Applicants' prior arguments regarding Krishnamurthy, and has not shown it to be in error. The Office has not identified any teaching of Krishnamurthy that teaches or suggests transmission of two streams of multiplexed video/audio stream, in accordance with Applicants' claim 10. If the Office believes that Applicants have misinterpreted this clear teaching of Krishnamurthy, or have missed other relevant teachings that support the position of the Office, Applicants respectfully request that the Office provide a specific and clear explanation of why Applicants' interpretation of Krishnamurthy is in error, with citation to supporting element(s) of figure(s), and specific column and line of Krishnamurthy.

Applicants respectfully maintain that Krishnamurthy does not teach or suggest, at least, "...[a] single-chip audio/video encoder device comprising, on a single integrated circuit: ... multiplexer circuitry that operates in a first mode and a second mode ... wherein the device transmits a first multiplexed stream to circuitry external to the device via a first output of the device; and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device."

The Office continues to assert that "...Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) comprising ... multiplexer circuitry that operates in a first mode and a second mode (col. 20, lines 22-25, "multi-channel mode" would obviously suggest a first mode and a second mode),...." *See* Office action of April 10, 2008 at page 3, Office action of October 16, 2008 at page 8. Applicants respectfully

disagree. Applicants again address the teachings of Krishnamurthy at column 20, lines 12-25, which is reproduced below, with the cited portion underlined:

> Each SSI serial input port 336 has three wires carrying a clock signal (sclk), a data signal (sdat), and a frame signal. All 24 clock signals sclk should be configured as the input clock signals and connected to an on-board 27-MHz clock oscillator 504. 27-MHz clock 504 will also be used as the DSP clock, and on-chip PLL circuits will generate a 90-MHz DSP clock. In that case, on-chip timers can be used for the PCR time-base corrections. The frame signals will indicate whether or not the data signal sdat carries meaningful data. The data signals sdat are burst with a maximum rate of 27 Mbps. The frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters.

The portion of Krishnamurthy shown above teaches that each "SSI serial input port 336" has "clock", "data", and "frame" signals as inputs, and that the "frame" signals will indicate whether the "data" signals carry meaningful data. Krishnamurthy also states that "...The frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters." The cited portion of Krishnamurthy, however, does not teach or suggest a "first mode" and "second mode" of a multiplexer, "...which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; **and** which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio;...", in accordance with Applicants' claim 10.

Applicants respectfully maintain that the "multi-channel mode" of Krishnamurthy is related to a "frame signal" used to "send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters...", and fails to

teach or suggest anything in regard to a "first mode" and "second mode" that relates to how "first compressed audio", "first compressed video", "second compressed audio" and "second compressed video" are multiplexed to form one or two multiplexed streams [wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device], in accordance with Applicants' claim 10. Therefore, Applicants' respectfully maintain that Krishnamurthy at column 20, lines 22-25 fails to teach at least this aspect of Applicants' claim 10.

In response to Applicants' argument of September 10, 2008, the Office states, in part, at pages 11-12:

> Krishnamurthy teaches a first MPEG-2 video encoder (320), a first audio encoder (322), a second MPEG-2 encoder (320n, 306n), a second audio encoder (322n, 306n), and a statistical multiplexing board (308), wherein the statistical multiplexing board (308 of fig. 3) is a multiplexing circuit for multiplexing the first encoded video signal and the first encoded audio signal (SSI, 328, 336), and the second encoded video signal and the second encoded audio signal (SSI, 328n, 336). The stat-mux (308 of fig. 3) can multiplex up to 24 channels of low delay MPEG-2 video/audio input bitstreams (SSI of fig. 3, col. 18, lines 50-52; col. 20, lines 10-11); and each SSI has three wires carrying a clock signal (sclk), a data signal (sdat), and a frame signal (col. 20, lines 12-13), and the frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters (col. 20, lines 22-25), so this is evidence to one of ordinary skill in the art to modify the stat-mux (308) of Krishnamurthy within a single chip for multiplexing the first encoded video and audio in a first mode and the second encode video and audio in a second mode.

(emphasis added)

Applicants respectfully submit that this response by the Office merely presents a restatement of Applicants' claim language, includes some text from Krishnamurthy that identifies elements of Krishnamurthy, and then offers only the conclusory statement that "...so this is evidence to one of ordinary skill in the art to modify the stat-mux (308) of Krishnamurthy within a single chip for multiplexing the first encoded video and audio in a first mode and the second encode video and audio in a second mode." Initially, Applicants respectfully note that Applicants' claim 10 does not recite "multiplexing the first encoded video and audio in a first mode and the second encode [sic] video and audio in a second mode," as suggested by the Office.

In addition, the Office fails to provide any explanation of why the simple laundry list of the elements of Krishnamurthy presented by the Office is "evidence to one of ordinary skill in the art to modify the stat-mux (308) of Krishnamurthy within a single chip". The Office does not explain how one of ordinary skill in the relevant art at the time of the invention would arrive at Applicants' claimed invention. For example, what is the source of a suggestion to create the subject matter of claim 10? The Office fails to provide any "...articulated reasoning with some rational underpinning to support the legal conclusion of obviousness..." or a "...clear articulation of the reason(s) why the claimed invention would have been obvious," which is recognized by M.P.E.P. §2142 to be "[t]he key to supporting any rejection under 35 U.S.C. 103." M.P.E.P. §2142 is clear, "...rejections on obviousness cannot be sustained with mere **conclusory** statements," such as those presented by the Office. Thus, for at least these reasons, and those presented during prior prosecution, Applicants respectfully submit that the Office has not established a *prima facie* case of obviousness, as required by M.P.E.P. §2142, that Krishnamurthy does not render Applicants' claim 10 unpatentable, and that claim 10 is allowable over Krishnamurthy.

The Office action of October 16, 2008 continues by asserting that Krishnamurthy teaches "...[a] single-chip audio/video encoder device ...which when operating in the first mode (308 of fig. 3, the multiplexer (308) for multiplexing up to 24 different channels of transport bitstreams from the MPEG-2 encoders; col. 20, lines 10-11) produces a first

multiplexed stream (fig. 5, multiplexing bitstreams and outputting a first multiplexed bitstream) from first compressed video (320 of fig. 3), first compressed audio (322 of fig. 3), second compressed video (ENCn, 320 of fig. 3), and second compressed audio (ENCn, 322 of fig. 3);...." *See* Office action of April 10, 2008 at page 3, Office action of Octobe 16, 2008 at page 8. Applicants again address Krishnamurthy at column 20, lines 1-11, which has been reproduced below in context, with the cited portion underlined:

> FIG. 5 shows a board-level block diagram of statistical multiplexing board 308 of computer system 300 of FIG. 3, according to one embodiment of the present invention. Stat-mux board 308 is a low-delay Input/Output (I/O) interface PCI board with the statistical multiplexing system and PCR time-base correction firmware. Stat-mux board 308 comprises an internal sub-system bus 502 configured with four Texas Instruments TMS320c5420 DSP chips 332, each having six SSI serial ports 336 and 512 Kbytes of on-chip SRAM memory 338, such that stat-mux board 308 can receive up to 24 different channels of transport bitstreams.

The cited portion of Krishnamurthy shown above simply teaches that an embodiment of a "stat-mux board 308" of Fig. 3 comprises four "TMS320c5420 DSP chips 332" each having six "SSI serial ports 336" and on-chip SRAM, so that "stat-mux board 308" can receive "...up to 24 different channels of transport streams." Applicants now turn to the alleged teachings of Fig. 5 of Krishnamurthy, which has been reproduced below:

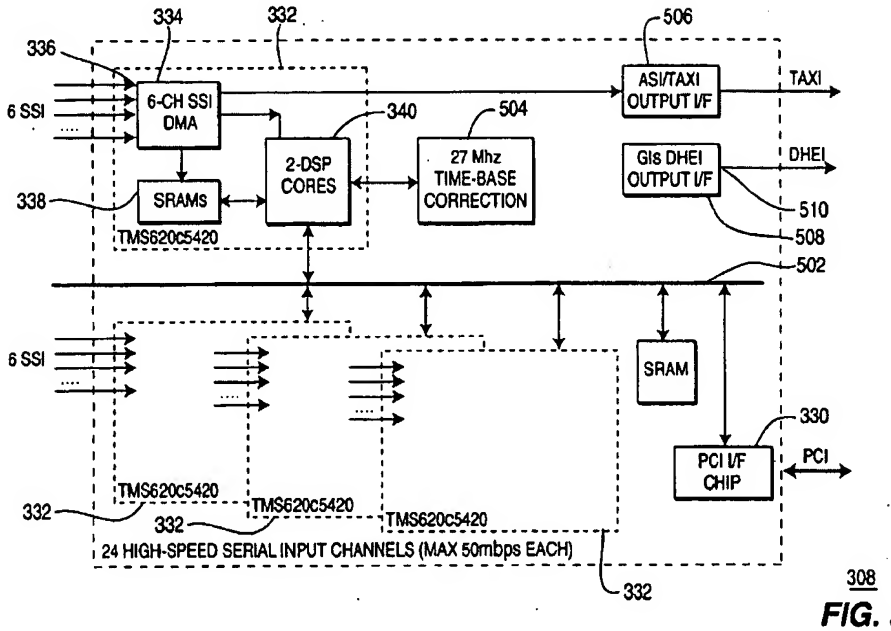

FIG. 5

The cited figure of Krishnamurthy reproduced above illustrates what Krishnamurthy describes as "...a board-level block diagram of the statistical multiplexing board of the computer system of FIG. 3." *See id.* column 4, lines 14-15. The illustration of Fig. 5 shows the "stat-mux board 308" with four "TMS320c5420 DSP chips 332" each having six "SSI serial ports 336", in which one of the "TMS320c5420 DSP chips 332" produces a signal to an element labeled as "ASI/TAXI OUTPUT I/F 506", which produces a signal labeled "TAXI". Krishnamurthy also shows an element "GIs DHEI OUTPUT I/F 508" producing a signal "DHEI 510". Krishnamurthy further describes the "stat-mux board 308" at column 18, lines 42-52, which recites:

> Stat-mux board 308 has a PCI bus interface 330 and four DSP chips 332, where each DSP chip 332 has a six-channel SSI DMA (Direct Memory Address) 334 with six SSI ports 336, SRAMs 338, two DSP cores 340, and an ASI/TAXI.TM. chip set from Advanced Micro Devices, Inc., of Sunnyvale, Calif., and, in block 342, a DHEI (Digital High-speed Expansion Interface) I/O port from General Instrument Corporation (GI) of Horsham, Pa., for GI's modulator and CA

> (Conditional Access) equipment. As such, stat-mux board 308 can support up to 24 channels of low-delay MPEG2 video/audio input bitstreams.

The portion of Krishnamurthy shown above simply repeats some of the teachings at column 20, lines 1-11, and in addition, states that an "ASI/TAXI chip set" and "DHEI I/O port" are provided on the "stat-mux board 308". Based on the above, Applicants respectfully submit that Fig. 5. of Krishnamurthy teaches the multiplexing of signals received on "SSI serial ports 336" to produce one "TAXI" output signal, used to transmit "...multiple compressed video streams over a **single**, shared communication channel...", as stated by Krishnamurthy at column 1, lines 15-19. This portion of Krishnamurthy does not, however, teach or suggest that "stat-mux board 308" of the "computer system" of Fig. 3 produces more than a single multiplexed stream of compressed audio and video for transmission by the "computer system" of Fig. 3, from the "...up to 24 different channels of transport bitstreams from the MPEG-2 encoders..." described in the portions and figures of Krishnamurthy, reproduced above.

The Office again asserts that Krishnamurthy teaches "...[a] single-chip audio/video encoder device ... which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio (SSI, 328 of fig. 3), and produces a second multiplexed stream (fig. 5, multiplexed bitstreams and outputting a second multiplexed bitstream) from the second compressed video and the second compressed audio (AUDIO ENC and MPEG-2 ENC of fig. 3);.... *See* Office action of April 10, 2008 at pages 3-4, Office action of October 16, 2008 at pages 8-9. Applicants respectfully disagree.

Applicants have shown above that Fig. 5 of Krishnamurthy does not teach or suggest that the "stat-mux board 308" produces more than one "TAXI" output stream, which Krishnamurthy teaches is used to transmit the multiplexed stream comprising multiple compressed video streams. While Krishnamurthy does disclose that the "encoder board 306" includes a "video encoder 320" ("MPEG-2 ENC" of Fig. 3), an

"audio encoder 322" ("AUDIO ENC" of Fig. 3), and a "DSP controller 326" with an "SSI port 328" (*See id.* at column 18, lines 34-41 and lines 56-60), Krishnamurthy does not teach or suggest that the "video/audio bitstream" transmitted from the "SSI port 328" of the "encoder board 306" is transmitted "...to circuitry external to the device..." via an "...output of the device...", in accordance with Applicants' claim 10. Instead, Krishnamurthy teaches that the output of "SSI port 328" of each "encoder board 306" is "...**directly** transmitted from the SSI port 328 of the corresponding encoder board 306 to an SSI port 336 on stat-mux board 308." (emphasis added) *See id.* at column 18, lines 56-60. Therefore, Applicants respectfully submit that Krishnamurthy does not teach or suggest, at least, Applicants' features "...[a] single-chip audio/video encoder device ... which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio ... wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device...", as asserted by the Office.

In response to Applicants' arguments of September 10, 2008, the instant Office action states, in part, at page 12:

> Krishnamurthy further teaches the stat-mux in figure 5 for outputting the multiplexed stream of the first encoded video and the first encoded video to circuitry external to the device (506, col. 20, lines 27-28), wherein the stat-mux (308 of fig. 5) would obviously output the multiplexed stream of the second encoded video and the second encoded audio to circuitry external to the device (506; col. 20, lines 27-28) via "TAXI", which is similar to the MUX (114 of fig. 5) of the present invention.

Again, the Office fails to provide any "...articulated reasoning with some rational underpinning to support the legal conclusion of obviousness...," does not explain how one of ordinary skill in the relevant art at the time of the invention would arrive at

Applicants' claimed invention, but simply offers the conclusory statement that the "stat-mux 308" of Krishnamurthy "...would obviously output the multiplexed stream of the second encoded video and the second encoded audio to circuitry external to the device." (emphasis added) As Applicants have shown above, Krishnamurthy teaches of outputting to an external device only one multiplexed stream, and does not teach or suggest outputting a single multiplexed stream of all audio and video in a one mode, and two different multiplexed streams of the audio and video in a second mode, as claimed. The simple unsupported statement by the Office that "the "stat-mux 308" would "...obviously output the multiplexed stream...to circuitry external to the device..." is insufficient, and does not meet the requirements of M.P.E.P. §2142. Therefore, Applicants respectfully submit that the Office has not met the requirements of M.P.E.P. §2142 to establish a *prima facie* case of obviousness, that Krishnamurthy does not render Applicants' claim 10 unpatentable, and that claim 10 is allowable over Krishnamurthy for at least the reasons set forth above, and during prosecution.

In addition, Applicants respectfully maintain that Krishnamurthy does not teach or suggest, at least, Applicants' feature "...[a] single-chip audio/video encoder device ... comprising: ... control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;...."

The Office action continues to assert that Krishnamurthy teaches "...[a] single-chip audio/video encoder device ... comprising: ... control circuitry (304 of fig. 3, note that the CPU (304) is programmable to control all elements, so the CPU would obviously synchronize all elements as described in figure 3) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;...." Applicants respectfully disagree.

Applicants respectfully maintain that Fig. 3 of Krishnamurthy fails to teach anything about "synchronizing". Applicants have reproduced Fig. 3 of Krishnamurthy again, below:

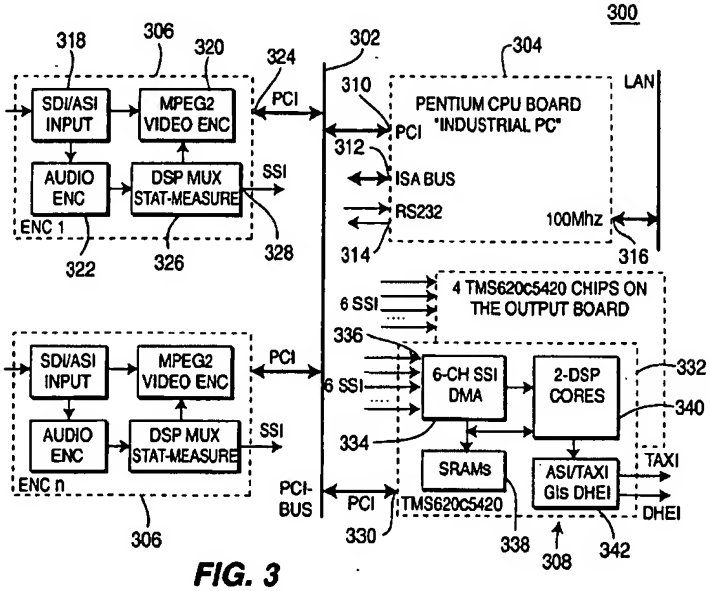

FIG. 3

Applicants respectfully repeat that Fig. 3 of Krishnamurthy simply teaches that Fig. 3 is "...a system-level block diagram of computer system, according to one embodiment of the present invention." *See id.* at column 4, lines 8-10. However, Applicants respectfully maintain that nothing in Fig. 3 teaches anything about "synchronization" of "encoders" and "multiplexer circuitry" by "control circuitry", in accordance with Applicants' claim 10.

Krishnamurthy describes Fig. 3 in greater detail at column 18, lines 9-19, which is reproduced again, below:

> FIG. 3 shows a system-level block diagram of computer system 300, according to one embodiment of the present invention. Computer system 300 is a PCI bus-based industrial PC (Personal Computer) enclosure with multiple PCI boards. In particular, computer system 300 comprises a PCI bus 302 configured with a Central Processing Unit (CPU) board 304, up to n=24 encoder boards 306, and a statistical multiplexing (stat-mux) board 308. Although computer system 300 relies on a PCI bus, it will be

> understood that any other suitable system bus could be used in alternative embodiments of the present invention.

Applicants again respectfully submit that there is nothing in this portion of Krishnamurthy that says anything about "synchronization" by "CPU board 304", or any other element of Fig. 3. of Krishnamurthy, of the other elements of the "computer system" of Fig. 3, which the Office has identified as teaching Applicants' "single-chip audio/video encoder device". **Applicants again respectfully note that the Office fails to provide any support for its conclusory statement that "...the CPU would obviously synchronize all elements as described in figure 3...."** (emphasis added) *See* Office action of April 10, 2008 at page 4, Office action of October 16, 2008 at page 9. In the absence of any support, Applicants are left to conclude that the Office is impliedly asserting that synchronization of the "encoder board 306" and "stat-mux board 308", which the Office identified as teaching Applicants' features "first encoder", "second encoder", and "multiplexer circuitry", by the "CPU board 304", is inherent.

According to MPEP §2112, Sec. IV, page 2100-54,55, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is **necessarily** present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, **may not be established by probabilities or possibilities**. The mere fact that a certain thing **may** result from a given set of circumstances **is not sufficient**.'" (emphasis added) In addition, M.P.E.P. §2112 recognizes that the courts have made clear that "In relying upon the theory of inherency, the examiner **must** provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic **necessarily** flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)." (emphasis in original).

Applicants respectfully maintain that the Office has failed to meet the requirements for an assertion of inherency, by providing a basis in fact and/or technical reasoning to reasonably support the determination that "...the CPU would obviously

synchronize all elements as described in figure 3..." **necessarily** flows from the teachings of the applied prior art. **If Applicants' statements are in error, Applicants respectfully request that the Office provide evidence of inherency as required by the M.P.E.P.** Therefore, Applicants respectfully submit that the Office has failed to show that (CPU board 304) would inherently synchronize the "encoder board(s) 306" and "stat-mux board 308" of the "computer system 300" of Krishnamurthy.

Indeed, Krishnamurthy clearly states, at column 10, line 60 to column 11, line 20:

> **Since the applications are not synchronized at the frame level, a frame-level target is computed for the encoder that will start encoding a frame next (at any given time)**, based on the average MQUANT chosen for that encoder. Using a rate-distortion model linking bit consumption, average MQUANT, and motion compensated distortion, and enforcing constraints on MQUANT, the bit count for a frame can be estimated from prior data. An example of the constraint on MQUANT can be that the quality is uniform across the applications, while ensuring that the temporal rate of change of average MQUANT is within a tolerance threshold. The channel bit rate is divided between the applications according to their respective complexities and relative significance. The complexities are updated on the fly, and the relative significance can be obtained from the results of off-line profiling stored in application profiles server 124.
>
> For the less controllable encoders, only the frame-level target (or average MQUANT) might be able to be communicated to the encoder. For the more controllable encoders, the basic unit of operation will be a slice (e.g., a row of macroblocks). **Because the encoders are not synchronized**, this will require a worst-case buffer requirement of 2 slices. A slice-level target is computed for each controllable encoder based on the frame target, the buffer fullness for that encoder (which is indicative of the buffer delay), and the instantaneous bit rate available after deducting the bits (within a latency window) from the less controllable encoders. The slice targets are also constrained by the fact that MQUANTs cannot change too much within a frame.

The statements by Krishnamurthy in the above text are clear.

If the Office did not mean to assert inherency, then Applicants respectfully submit that the Office has failed to provide any basis or support for its conclusory statement of the obviousness of this aspect of Applicants' claim 10. Applicants again respectfully point out that M.P.E.P. §2142 notes the clear opinion of the Federal Circuit that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." Applicants respectfully submit that the Office has failed to provide such an "... articulated reasoning with some rational underpinning to support the legal conclusion of obviousness...", required by the courts. Further, M.P.E.P. §2142 states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." (emphasis added) However, no such "...articulation of the reason(s) why the claimed invention would have been obvious..." has been provided by the Office to support the rejection of this aspect of Applicants' claim 10.

Therefore, Applicants respectfully submit that the Office has failed to show how and why Krishnamurthy teaches that the encoders (i.e., "video encoder 320" of Fig. 3) of the "computer system 300" of Krishnamurthy are synchronized and, therefore, that it is not true that Krishnamurthy teaches that the "CPU board 304" of Krishnamurthy teaches "...control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;...", as recited by Applicants' claim 10. Applicants respectfully submit that Krishnamurthy does not teach or suggest at least this aspect of Applicants' claim 10.

In response to Applicants' arguments of September 10, 2008, the instant Office action states, in part, at pages 12-13:

> Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, or harmonize all operations of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for

> all circuits properly working. Since Krishnamurthy teaches the MPEG-2 encoder chip that would obviously has a control function to synchronize the multiplexer, audio and video encoders according the MPEG-2 standards, therefore one of ordinary skill in the art to modify the control function according to MPEG-2 into the CPU (304 of fig. 3) to perform synchronization. In view of the discussion above, the claimed features are unpatentable over Krishnamurthy.

Applicants respectfully submit that a teaching by Krishnamurthy that "Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3" is insufficient to establish a *prima facie* case that "...the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, or harmonize all operations of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuits properly working." Indeed, as Applicants have previously shown that Krishnamurthy teaches, in the portion of Krishnamurthy reproduced above from column 10, line 60 to column 11, line 20, "...[s]ince the applications are not synchronized at the frame level, a frame-level target is computed for the encoder that will start encoding a frame next (at any given time)." (emphasis added) Krishnamurthy, as at column 10, line 60 to column 11, line 20, also clearly states that "...the encoders are not synchronized."

Also in response to Applicants response filed September 10, 2008, the Office states the following, at page 13:

> In response to applicant's argument of the obviousness, the examiner would like point out the following **basic principle of a proper prior art analysis within 35 U.S.C. 103(a).**
>
> Not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. In re Preda, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and In re Shepard, 319 F.2d 194,138 USPQ 148 (CCPA 1963). Skill in the art is presumed. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir.1985). Furthermore,

> artisans must be presumed to know something about the art apart from what the references disclose. In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962).
>
> The obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Boze 416 F.2d 1385,163 USPQ 545 (CCPA 1969)). Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. In re Bode, 550 F.2d 656,193 USPQ 12 (CCPA 1977).

(bold added, underline in original)

Applicants respectfully note that according to M.P.E.P. §2142, "[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." Further, Applicants respectfully submit that, in regard to a "proper prior art analysis within 35 U.S.C. 103(a)", M.P.E.P. §2142 states that "[t]he Supreme Court in *KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007), 82 USPQ2d 1385, 1396 noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made **explicit**." As previously noted above, the Office fails to make the analysis explicit, and fails to provide the "... articulated reasoning with some rational underpinning to support the legal conclusion of obviousness...", required by the court. Further, M.P.E.P. §2142 states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." The Office fails to provide such "clear articulation" or "explicit analysis".

With regard to dependent claim 15, Applicants respectfully maintain that claim 15 recites, in part, "...wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device,...." The Office again asserts that "...Krishnamurthy further teaches wherein the device comprises at least one bus interface (PCI, 302 and 310 of fig. 3) that

is configurable to operate to couple the control circuitry (304 of fig. 3) and at least one controller external (316 of fig. 3, downloading micro-codes for MPEG-2 encoder chip, 306 of fig. 3, col. 19, lines 22-28) to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals (PCI of fig. 3)." *See* Office action of April 10, 2008 at page 5, Office action of October 16, 2008 at pages 9-10. Applicants respectfully disagree. Applicants respectfully note that the Office cites only Krishnamurthy as teaching the features of Applicants' claim 15.

Applicants respectfully maintain that the Office previously identified the "computer system 300" and the "CPU board 304" of Fig. 3 of Krishnamurthy as teaching Applicants' "single-chip audio/video encoder device" and "control circuitry" of Applicants' claim 10. Applicants respectfully maintain that the Office also now identifies "PCI Bus 302" and "LAN interface 316" as teaching Applicants' "at least one bus interface" and "at least one controller external to the device" of Applicants' claim 10. Applicants respectfully submit that it is clear to one of ordinary skill in the relevant art after only a brief review of Fig 3, that the "PCI Bus 302" does not operate to couple the "CPU board 304" to the "LAN interface 316". Indeed, Krishnamurthy explains, at column 18, lines 20-26, that the "CPU board 304" has "...a (e.g., 100-MHz) Local Area Network (LAN) interface 316..." Further, Applicants respectfully submit that a "LAN interface 316" is different from and does not teach Applicants' feature "at least one controller." Because the "LAN interface 316" is part of the "CPU board 304", and Krishnamurthy does not teach that the "LAN interface 316" is connected to the "PCI Bus 302", Applicants respectfully submit that "PCI Bus 302" does not operate to couple the "CPU board 304" and the "LAN interface 316", in accordance with Applicants' claim 15. Therefore, Applicants respectfully submit that Krishnamurthy does not teach or suggest at least "...wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device,...", as recited by Applicants' claim 15.

Applicants respectfully note that, although the Office repeats the rejection of claim 15 verbatim, the Office has failed to respond to Applicants' arguments

regarding the rejection of claim 15 of the Office action of April 10, 2008, as set forth by the Applicants in the response file September 10, 2008. Thus, the Office has not overcome Applicants' arguments and claim 15 should be allowable for at least this reason.

Based at least upon the above, Applicants respectfully submit that the Office has failed to establish a *prima facie* case of obviousness, as required by M.P.E.P. §2142, and that Krishnamurthy does not teach, suggest, or otherwise render Applicants' claim 10 unpatentable. Further, Applicants respectfully submit that the Office has also failed to show how and where Krishnamurthy teaches or suggests Applicants' claim 15.

Therefore, Applicants respectfully submit that claim 10 is allowable over Krishnamurthy, for at least the reasons set forth above. Because claims 11-23 depend from allowable independent claim 10, Applicants respectfully submit that Krishnamurthy does not render any of claims 11-23 unpatentable, and that claims 11-23 are also allowable over Krishnamurthy. Further, Applicants have shown above that claim 15 is independently allowable over Krishnamurthy. Accordingly, Applicants respectfully request that the rejection of claims 10-12, 15-16, and 20 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

With regard to independent claim 24, Applicants respectfully submit that claim 24 recites limitations similar to those of independent claim 10, and was rejected on the same grounds as independent claim 10, citing the same teachings of Krishnamurthy as those used in the rejection of claim 10. Therefore, Applicants respectfully submit that claim 24 is allowable over Krishnamurthy for at least the reasons set forth above in Applicants' response to the rejection of claim 10. Because claims 25-36 depend either directly or indirectly from independent claim 24, Applicants respectfully submit that claims 25-36 are also allowable over Krishnamurthy, for at least the same reasons. Further, dependent claim 28, which depends from claim 24, was rejected for the same reasons as Applicants' claim 15, which Applicants have shown above is independently

allowable. Accordingly, claim 28 is independently allowable over Krishnamurthy. Applicants respectfully request, therefore, that the rejections of claims 24-25, 28-29, and 33 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

V. The Proposed Combination Of Krishnamurthy And Bruck Does Not Render Claims 13 And 26 Unpatentable

Claims 13 and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Bruck. Applicants respectfully submit that claims 13 and 26 depend, respectively, from independent claims 10 and 24. Applicants respectfully maintain that claims 10 and 24 are allowable over the proposed combination of references, in that Bruck fails to overcome the deficiencies of Krishnamurthy set forth above. Because independent claims 10 and 24 are allowable over the proposed combination of Krishnamurthy and Bruck, Applicants respectfully submit that claims 13 and 26 that depend therefrom, are also allowable, for at least the same reasons. Accordingly, Applicants again respectfully request that the rejections of claims 13 and 26 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

VI. The Proposed Combination Of Krishnamurthy And Hinchley Does Not Render Claims 14, 17-19, 27, And 30-32 Unpatentable

Claims 14, 17-19, 27, 30-32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Hinchley. Applicants respectfully submit that claims 14 and 17-19, and claims 27 and 30-32 depend, respectively, from independent claims 10 and 24. Applicants respectfully maintain that claims 10 and 24 are allowable over the proposed combination of references, in that Hinchley fails to overcome the deficiencies of Krishnamurthy set forth above. Because independent claims 10 and 24 are allowable over the proposed combination of Krishnamurthy and Hinchley, Applicants also respectfully submit that claims 14, 17-19, 27, and 30-32, that depend therefrom, are also allowable, for at least the same reasons.

Further, with regard to claims 14, 17, 27, and 30, Applicants respectfully submit that claims 14 and 27 recite, in part, "...wherein the device comprises at least one

interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data...", while claims 17 and 30 recite, in part, "...wherein the at least one bus interface is configurable to act as a bus master using direct memory access."

Applicants respectfully note that the Office has not addressed Applicants' arguments of September 10, 2008.

Based at least upon the above, Applicants respectfully submit that the Office has failed to establish a *prima facie* case of obviousness, as required by M.P.E.P. §2142, and that claims 14, 17-19, 27, and 30-32 are allowable over Krishnamurthy and Hinchley. Accordingly, Applicants respectfully request that the rejections of claims 14, 17-19, 27, and 30-32 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

VII. The Proposed Combination Of Krishnamurthy And Boice Does Not Render Claims 21-23 And 34-36 Unpatentable

As an initial matter, Item 10 of the Office action (*See id.* page 16) rejects claims 21-22 and 34-35 over Krishnamurthy and Boice. The detailed discussion of the rejection, however, begins by addressing claims 21-23 and 34-36, but then recites language that does not appear to be the language of claims 21-22 and 34-35. Applicants are unable to determine what rejection was intended.

Notwithstanding, Applicants respectfully submit that claims 21-22 (or 21-23) and 34-35 (or 34-36) depend, respectively, from independent claims 10 and 24. Applicants respectfully submit that claims 10 and 24 are allowable over the proposed combination of references, in that Boice fails to overcome the deficiencies of Krishnamurthy set forth above. Because independent claims 10 and 24 are allowable over the proposed combination of Krishnamurthy and Boice, Applicants respectfully submit that claims 21-23 and 34-36 that depend therefrom are also allowable, for at least the same reasons.

Further, with respect to claims 22, 23, 35, and 36, Applicants respectfully submit that claims 22 and 35 recite, in part, "...wherein the plurality of search processors operate in parallel, each upon a different portion of a macroblock...", while claims 23

and 36 recite, in part, "...wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a plurality of resolutions." Applicants respectfully submit that the proposed combination of Krishnamurthy does not teach or suggest at least these features of Applicants' claims 22, 23, 35, and 36.

The Office admits that Krishnamurthy does not disclose "...each of motion estimation processors comprises a plurality of search processors that operate in parallel upon a single macroblock, and each search processor operating at a different one of a plurality of resolutions (scaling or half pixel search, quarter pixel search) as claimed." *See* Office action of April 10, 2008 at page 7, Office action of October 16, 2008 at page 16.

The Office then relies upon Boice, and states that "...Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors sub-dividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of resolutions (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3)." Applicants respectfully disagree with what Boice allegedly teaches. The Office does not explain how and why the cited portions of Boice teach what is alleged.

Applicants respectfully submit that Boice makes no mention of "resolution", let alone "half pixel search" and "quarter pixel search", as alleged by the Office. Instead, Boice states the following, at column 4, line 66 to column 5, line 21:

> **The process of searching for a best match involves analyzing each unique 16 x 16 rectangular grid of pixels contained within the bounds of the search window in the reference frame.** By example, an 80 x 80 search window would contain 4225 unique 16 x 16 pixel grids. **Each grid contained in the window is analyzed in raster scan order by starting in the upper leftmost corner of the window, obtaining a search result, and moving one pixel row to the right to obtain a second**

> **search result.** The process is repeated in successive rows in the window. At each grid position in the search window a computation or search result is performed which involves summing the absolute difference between the luminance pixel values in the macroblock currently being encoded, macroblock 30 in frame 22 in the present example, and the corresponding luminance pixel values of the 16 x 16 pixel grid currently being analyzed. There is a one to one correspondence between the number of unique 16 x 16 grids contained within the search window and the number of search results computed. It is apparent that utilizing an extended window 36 affords a greater number of search results as a consequence of the extended window covering additional pixel grids. The probability of obtaining a more optimal best match motion vector is enhanced as a result.

Applicants have searched Boice and have been unable to identify any teaching related to searching at "half pixel" and "quarter pixel" resolutions, as alleged by the Office. **If Applicants have inadvertently overlooked such a teaching, Applicants respectfully request that the Office identify such teachings by specific citation to column/paragraph and line, and provide a specific and detailed explanation of how and why the cited teachings allegedly disclose Applicants' claimed features.**

In addition, the Office cites elements "36", "38", and "40" of Fig. 3 of Boice as teaching Applicants' claims. Fig. 3 of Boice is reproduced below:

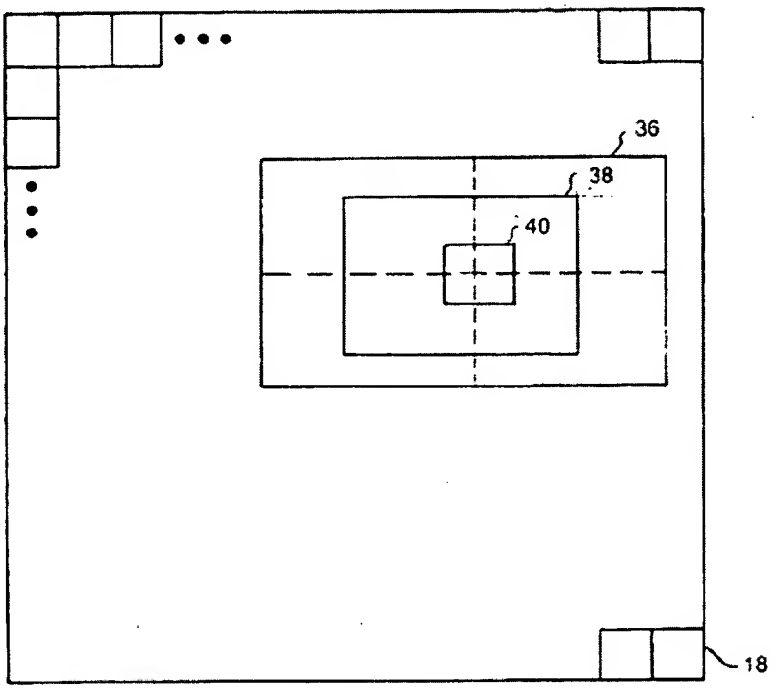

Fig. 3

Applicants respectfully submit that the elements having reference characters "36" and "38" are described by Boice as "extended window 36" and "single encoder configuration window 38". The disclosure of Boice fails to even make reference to an element in Fig. 3 having the reference character "40". While Boice does make reference to element "42", which Boice indentifies as "reference macroblock 42", Boice does not teach or suggest that the "extended window 36", "single encoder configuration window 38", and "reference macroblock 42" represent anything related to "...wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a plurality of resolutions." Further, the Office has failed to provide a "...some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness...", and instead offers only conclusory statements pointing not to specific portions of the text of Boice, but rather to elements in the figures, without explanation or interpretation.

Applicants respectfully note that, although the Office repeats the rejection of claims 21-23 (or 21-22) and 34-35 (or 34-36), the Office has failed to address Applicants' arguments regarding the rejection of claims 22, 23, 35, and 36 of the Office action of April 10, 2008, as set forth by the Applicants in the response file September 10, 2008. Thus, the Office has not overcome Applicants' arguments and those claims should be allowable for at least this reason.

Therefore, for at least the reasons set forth above, Applicants respectfully submit that the Office has failed to establish a *prima facie* case of obviousness, as required by M.P.E.P. §2142, that the proposed combination of Krishnamurthy and Boice does not teach, suggest, or otherwise render claims 22, 23, 35, and 36 unpatentable, and that claims 22, 23, 35, and 36 are allowable over Krishnamurthy and Boice.

Based at least upon the above, Applicants respectfully submit that claims 21-22 (or 21-23) and 34-35 (or 34-36) are allowable over Krishnamurthy and Boice. Accordingly, Applicants respectfully request that the rejections of claims 21-23 and 34-36 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

VIII. The Proposed Combination Of Krishnamurthy, Boice, And Kopet Does Not Render Claims 21-22 And 34-35 Unpatentable

As an initial matter, Item 11 of the Office action (*See id.* page 17) rejects claims 21-22 and 34-35 over Krishnamurthy, Boice, and Kopet. Applicants respectfully note that claims 21-22 and 34-35 were rejected in Item 10 of the instant Office action (See id. at page 15) over Krishnamurthy and Boice. The detailed discussion of the rejection, however, begins by addressing claim 23. Applicants are unable to determine what rejection was intended.

Notwithstanding, Applicants respectfully submit that claim 23 depends from independent claim 10. Applicants respectfully submit that claim 10 is allowable over the proposed combination of references, in that Kopet fails to overcome the deficiencies of Krishnamurthy and Boice, set forth above. Because independent claim 10 is allowable

over the proposed combination of references, Applicants respectfully submit that claim 23 that depends therefrom is also allowable, for at least the same reasons.

Conclusion

In general, the Office has made various statements regarding the claims in the Application and the cited references, which are now moot in light of the above. Thus, Applicants will not address such statements at the present time. However, Applicants expressly reserve the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

The Applicants believe that all of claims 10-36 define allowable subject matter, and request that the Application be passed to issue. Should the Examiner disagree or have any questions regarding this submission, Applicants respectfully invite the Examiner to telephone the undersigned at (312) 775-8000 to resolve any outstanding issues.

A Notice of Allowability is courteously solicited.

The Commissioner is hereby authorized to charge the fee required under 37 C.F.R. §1.17(a)(3) for the extension of time, and any additional fees required by this submission, or to credit any overpayments, to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Dated: April 16, 2009

By: /Kevin E. Borg/
Kevin E. Borg
Reg. No. 51,486

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(tel) 312-775-8000
(fax) 312-775-8100